13.1 Immediate addressing: The value of the operand is in the instruction.

13.2 Direct addressing: The address field contents the effective address of the operand

13.3 Indirect addressing: The address field refers to the address of a word in memory,  
which in turn contains the effective address of the operand.

13.4 Register addressing: The address field refers to a register that contains the  
operand.

13.5 Register indirect addressing: The address field refers to a register, which in turn  
contains the effective address of the operand.

13.6 Displacement addressing: The instruction has two address fields, at least one of  
which is explicit. The value contained in one address field (value = A) is used  
directly. The other address field refers to a register whose contents are added to A  
to produce the effective address.

13.7 Relative addressing: The implicitly referenced register is the program counter  
(PC). That is, the current instruction address is added to the address field to  
produce the EA.

13.8 It is typical that there is a need to increment or decrement the index register after  
each reference to it. Because this is such a common operation, some systems will  
automatically do this as part of the same instruction cycle, using autoindexing.

13.9 difference: These are two forms of addressing, both of which involve indirect addressing and ndexing. With preindexing, the indexing is performed before the indirection.  
With postindexing, the indexing is performed after the indirection.

13.10 Number of addressing modes.  
Number of operands: Typical instructions on today's machines provide for two operands.  
Register versus memory: The more that registers can be used for operand references, the fewer bits are needed.  
Number of register sets: More the Better  
Address range: This matters  
Address granularity.

13.11 Advantages: It easy to provide a large repertoire of opcodes, with different  
opcode lengths. Addressing can be more flexible, with various combinations of  
register and memory references plus addressing modes.  
Disadvantages: an increase in the complexity of the CPU.